Matthias Wenzl

Curriculum Vitae

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Education

2018– today **ongoing**, *Vienna University of Technology*.
Doctorate Computer Science

2010–2012 **Mag.rer.soc.oec.**, *Vienna University of Technology*.
Master Computer Science Management

2008–2011 **Dipl. Ing.**, *Vienna University of Technology*.
Master Computer Engineering

2004–2008 **Bsc.**, *Vienna University of Technology*.
Bachelor Computer Engineering

1994–2003 **Matura**, *Grammar School Friesgasse, 1150 Vienna*.

Experience

09/2019– today **Senior Researcher**, *FH Technikum Wien*, Vienna.
Context: Embedded Systems Security

- Requirements definition, design & Implementation of a bare bare metal and RTOS aware run-time based dataflow analysis framework for ARM based SoCs and MCUs in the context of project ISaFe.
- Assets:
  - ARM MCUs, Bare Metal, RTOS (Free RTOS, TI-RTOS), Linux, QEMU
  - Python, C++, C, Assembler(ARM)
  - Make, CMake, Git

07/2019– today **Technical Project manager**, *FH Technikum Wien*, Vienna.
Context: Embedded Systems Security

- Guidance of one junior researcher in the context of project AutoHoneyI(I)oT.
- Performed architecture and code reviews
- Financial and technical reporting

09/2014– 08/2019 **Technical Project Manager**, *FH Technikum Wien*, Vienna.
Context: Embedded real-time applications

- Guidance of one junior researcher in the context of project DIScoVER
- Performed architecture and code reviews
- Financial and technical reporting
- Requirements definition, design & Implementation of the following embedded real-time applications in the context of project DIScoVER.
  - MCU based civil flight radar receiver (ADS-B)
  - SDR based civil flight radar transmitter (ADS-B)
  - MCU based civil flight radar transmitter (ADS-B)
  - MCU based finger print verification unit
- Assets:
  - ARM MCUs, Bare Metal, RTOS (TI-RTOS), Linux, Embedded Linux (Yocto), SDR, GnuRadio
  - Python, C++, C, Matlab, UML, SysML
  - Make, CMake, Git

05/2013– 08/2014 **Senior Researcher**, *FH Technikum Wien*, Vienna.
Context: Hardware Runtiume Verification in saftey relevant environments

- Requirements definition, design & Implementation of an assertion synthesis test bed.
  - FPGA based multi-core design (SPARCv8)
  - Firmware development including bootloader for SPARCv8
- Requirements definition, design & Implementation of a prototypic PSL to VHDL assertion synthesis compiler.
- Assets:
  - FPGA (Altera), Bare Metal,
  - C, Assembler (SPARCv8), VHDL, PSL, UML, SysML
  - Make, SVN

06/2011– 08/2013 **Technical Project Manager**, *FH Technikum Wien*, Vienna.
Context: System level simulation for heterogeneous embedded multi-core platforms

- Guidance of two junior researchers in the context of project DEVPATS.
- Performed architecture and code reviews
- Financial and technical reporting
- Requirements definition, design & implementation of a framework for generating heterogeneous multi-core system level simualtion platforms from device tree desription and available simulation models
- Assets:
  - QEMU, SimSoC (SystemC based system Level emulation)
  - C, C++, SystemC, Assembler (ARM, PowerPC), Embedded Linux (Buildroot), uCLinux
  - Make, SVN

09/2010 - 05/2011 **Junior Researcher**, *FH Technikum Wien*, Vienna.
Context: System level simulation for heterogeneous embedded multi-core platforms

- Evaluation of system level simulation platforms for heterogeneous embedded multi-core systems.
- Assets:
  - QEMU, SimSoC (SystemC based system Level emulation)
  - C, C++, SystemC, Assembler (ARM, PowerPC), Embedded Linux (Buildroot), uCLinux
  - Make, SVN

07/2008 - 04/2009 **Junior Hardware Engineer**, *Gleichmann Electronic Research GmbH*, Hagenberg.
*Context:*IP-Core development & verification in VHDL

- Implementation & verification of IP-Cores in VHDL for FPGAs (GPIO, 16550 compliant UART, CAN2.0)
- Assets:
  - VHDL, TCL
  - Modelsim
  - Altera Quartus II

2005 - 2007 **Internships**, *Siemens AG Austria*, Vienna.
Context: Software development.

- Implementation of a formatted text file to latex generator in Perl
- Implementation of a sensor node monitoring tool in Perl/GTK
- Implementation of an authentication plugin for a sensor node monitoring tool in C
- Assets:
  - Perl
  - C
  - GTK

Languages

German Mother tongue

English fluent

Key skills

- Embedded firmware development
- Design & development of Real-Time systems
- Device driver development for RTOS and Embedded Linux
- Setup & configuration of cross build environments
- Requirement analysis and system architecture
- Deep understanding of the tight software/hardware entanglement of FPGA based applications
- Elaborate communication skills
- Guidance of junior employees
- Teamwork

Won research grants

- FFG Bridge-1 funded project ISaFe - Volume: EUR 330.000
- FFG Bridge-1 Young Scientists funded project AutoHoneyI(I)oT - Volume: EUR 300.000
- MA23 City of Vienna funded project DIScoVER - Volume: EUR 560.000

Publications

[1] Wenzl M. Merzdovnik G. Weippl E. Isafe - injecting security features into constrained embedded firmware. *ERCIM News*, Volume 2019(119):25–26, 2019.

[2] Wenzl M. Merzdovnik G. Ullrich J. and Weippl E. From hack to elaborate technique - a survey on binary rewriting. *ACM Computing Surveys (CSUR)*, 52(3):49:1–49:37, 2019.

[3] Wenzl M. Rössler P. and Puhm A. Checking application-level properties using assertion synthesis. In *Proceedings of the ASME/IEEE International Design Engineering Technical Conferences & Computers and Information in Engineering Conference*, page 9, Anaheim CA. USA, August 2019.

[4] Wenzl M. Kluka D. Adding channel security to a fingerprint verification chain. In *Proceedings of 13th ASME/IEEE International Conference on Mechatronic & Embedded Systems & Applications (MESA)*, Cleveland Ohio USA, August 2017.

[5] Taucher H. Matschnig M. Wenzl M. Fibich C. Rössler P. Logic synthesis of assertions for saftey-critical applications. In *Proceedings of the 2015 International Conference on Industrial Technology (ICIT)*, page 6, March 2015.

[6] Schefer-Wenzl S. Wenzl M. Roboter mit Himbeeren, Ein Überblick über Roboterbausätze und GPIO Bibliotheken auf Raspberry Pi (2). *Entwickler Magazin*, pages 64–68, June 2015.

[7] Wenzl M. Schefer-Wenzl S. Ran an den Knochen: Java Embedded auf dem Beagle Bone. *Entwickler Magazin Spezial "Internet of Things"*, pages 93–97, 2014.

[8] Fibich C. Wenzl M. Rössler P. On automated generation of checker units from hardware assertion languages. In *Proceedings of the Microelectronic Systems Symposium 2014 (MESS'14)*, May 2014.

[9] Wenzl M. Schuster H. Obermayer C. Balog P. Embedded multi core virtual prototyping for software engineers. In *Proceedings of the ASME 2013 International Design Engineering Technical Conferences and Computers and Information in Engineering Conference (IDETC/CIE)*, Portland Oregon USA, August 2013.

[10] Wenzl M. Schefer-Wenzl S. Java Embedded auf dem Beagle Bone. *Java Magazin*, (7):86–91, 2013.

[11] Wenzl M. Evaluating best practices for teaching multi-core programming. In *Ireland International Conference on Education (IIEC-2012)*, Dublin Ireland, October 2012.

[12] Schuster H. Wenzl M. Zauner M. A framework for teaching embedded multi-core programming. In *Proceedings of the 8th IEEE/ASME International Conference on Mechatronic and Embedded Systems and Applications*, pages 292–297, Suzhou China, July 2012.