About Martin Trojer

Martin Trojer studied electrical engineering at the Technical University of Graz, where he also completed his Ph.D. focusing on low-noise, high-speed analog video frontends. Over a 25-year career in the semiconductor industry, he advanced and applied his expertise in analog and mixed-signal IC design at global tech leaders including Siemens, Infineon, Micronas, Lantiq, and Intel. Throughout these roles, he drove the development of pioneering data converter topologies and digital calibration techniques. Following a tenure as Senior Engineering Manager at MaxLinear, he joined IMS Nanofabrication GmbH in 2024. Today, he serves as Project Manager, leading the analog chip design for cutting-edge multi-beam maskwriting tools used in advanced global semiconductor manufacturing. Dr. Trojer holds several patents, received an IEEE conference paper award, and frequently mentors graduate academic research.

Biographical Sketch: Dr. techn. Martin Trojer

A. Contact & Current Position

- **Name:** Martin Trojer, Dr. techn. Dipl.-Ing.
- **Current Position:** Project Manager / Analog Chip Design Engineer
- **Institution/Company:** IMS Nanofabrication GmbH, Austria
- **Email:** martin.trojer@ims.co.at

B. Personal Statement

Dr. Martin Trojer is a highly accomplished Analog and Mixed-Signal (MS) IC Design Expert and Project Manager with over 25 years of experience in the semiconductor industry. His core expertise spans advanced analog chip design for state-of-the-art semiconductor manufacturing equipment, system-level specification, and the digital calibration of high-speed, high-resolution converters. He has a proven track record of driving technical excellence and people leadership within leading global tech firms and cutting-edge nanotechnology enterprises.

C. Education & Training

- **2007 – 2010: Dr. techn.** (Ph.D. equivalent) in Electrical Engineering, Technical University of Graz, Austria
    - *Thesis:* Low Noise High Speed Analog Video Frontends for PC and HDTV Applications in 90nm and 65nm
- **1992 – 1998: Dipl.-Ing.** (M.Sc. equivalent) in Electrical Engineering, Technical University of Graz, Austria

- *Thesis:* Realization study of different A/D and D/A converter topologies for high-speed data modems

D. Positions & Employment

- **April 2024 – Present:** Project Manager / Analog Chip Design, *IMS Nanofabrication GmbH*
  - Responsible for the Analog Chip Design of the cutting-edge Multi-Beam Maskwriting Tool (MBMW) used by major global chip manufacturers.
- **2020 – March 2024:** Senior RF/MS IC Design Engineering Manager / Team Lead, *MaxLinear Ltd.*
  - IP lead of an RF single-slice ADC, including digital calibration, top-level integration, and system specification. Managed university cooperation
- **2015 – 2020:** Analog Engineer / Project & People Manager, *Intel*
  - IP lead for high-resolution Time-Interleaved (TI) pipeline ADCs and design of MS circuits (comparators, reference buffers, clock gen)
- **2009 – 2015:** Mixed Signal Design Engineer, *Lantiq A Ltd*
  - Developed TI SAR ADCs for ethernet applications and designed on-chip process monitors
- **2002 – 2008:** Mixed Signal Design Engineer, *Micronas*
  - Designed mixed-signal circuits for video applications and authored key patents.
- **1998 – 2002:** Analog- and Mixed-Signal Design Engineer, *Siemens / Infineon Villach Design Center*
  - Engineered mixed-signal analog designs for ISDN and ADSL modems

E. Honors, Patents & Professional Memberships

- **Patents:** Granted patents on determining RC time constants of on-chip resistors and capacitors
- **Awards:** Recipient of a *Paper Award* at the international IEEE PRIME conference
- **Publications:** Authored a paper on pipelined ADCs accepted for an internal Intel conference; regular lecturer and attendee at IEEE conferences
- **Memberships:** Active member of the *IEEE Solid-State Circuits Society (SSCS)*
- **Mentoring:** Supervised academic graduate work, including a TU Graz diploma is on Low-Power 12-Bit Pipeline ADCs