

Conference Program

09:00 – 09:30 Registration & Welcome Coffee

09:30 – 09:40 Conference Opening

09:40 – 10:25 Keynote Address

Electron Multibeam Mask Writing for Leading-Edge Chip Manufacturing
Martin Trojer, Hans Löschner and Elmar Platzgummer
IMS Nanofabrication GmbH

10:25 – 10:45 Coffee Break

10:45 – 12:05 Paper Session Digital Systems & Design Automation

Session Chair: *tba*

- 10:45 From Annotated C to a CGRA Benchmark: An Automation Toolchain for HEEpsilon
Sebastian Wiedemann
Technische Universität Wien
- 11:05 Design Automation Methodology of Synchronous SAR ADC
Hanif Khan, Philipp Sommeregger, Wolfgang Scherr, Christoph Bodner, Violeta Petrescu, Santiago Martin Sondon and Johannes Sturm
Carinthia University of Applied Sciences
- 11:25 Automated Schematic-to-Netlist Conversion and Analog Circuit Structure Recognition
Jaipriya Narahari, Ghilas Kahlouche, Santiago Sondon, Matthew Bio and Johannes Sturm
Carinthia University of Applied Sciences
- 11:45 Zero-Overhead SEU Mitigation for AMD 7 Series FPGAs via Configuration Patching
Christian Fibich, Martin Horauer and Roman Obermaisser
University of Applied Sciences Technikum Wien, University of Siegen

12:05 – 13:05 Lunch

13:05 – 14:25 Paper Session Analog Design

Session Chair: *tba*

- 13:05 Input Current Compensation Scheme for Area and Power Efficient Optical Receiver Frontends
Christoph Gasser and Horst Zimmermann
AIT Austrian Institute of Technology, Technische Universität Wien
- 13:25 Automated Sizing of a Folded-Cascode OTA Using a Python-Based Framework
Shyam Sunder Mandapally, Violeta Petrescu, Philipp Sommeregger, Christof Bodner, Wolfgang Scherr, Santiago Martin Sondon, Johannes Sturm and Matthew Bio
Carinthia University of Applied Sciences
- 13:45 A Framework for gm_{id}-Based Analog Sizing via Reusable Building Blocks
Arjun Ganesh, Giovanni Dalla Colletta and Peter Thurner
Infineon Technologies, Johannes Kepler Universität
- 14:05 Current Reuse Technique Employing a Class-D Oscillator for Low-Power RF Receivers
Mohammad Niazi, Hassan Hedayat Zadeh Ganji, Harald Pretl, Reinhard Feger and Saeed Saeedi
Johannes Kepler Universität Linz, Tarbiat Modares University

14:25 – 14:40 Poster Pitch Session

Session Chair: *tba*

- 14:25 Beamforming in Coherent Radar Networks Under Array Mismatch in Arbitrary Geometries
Michael Preining, Mayeul Jeannin and Reinhard Feger
Johannes Kepler University Linz, Infineon Technologies Austria AG
- 14:30 Lessons Learned from Using Commercial Electromagnetic Shielding for Side-Channel Analysis

Michael Hutter and Carlos Andres Lara-Nino
Universität der Bundeswehr München & PQShield

14:35 Automated RTL Abstraction Lifting for Model-Driven Structural Exploration
You-Jen Chang, Mohamed Badawy, Paritosh Kumar Sinha, Juntian Yang and Wolfgang Ecker
Infineon Technologies AG

14:40 – 15:10 Poster Viewing & Coffee Break

Extended break: visit the posters and meet the authors

15:10 – 16:30 Paper Session Analog & RF Design

Session Chair: *tba*

15:10 Finger Count Effects in MOSFET Lookup Tables for Analog Circuit Sizing
Amith Nanjesh, Wolfgang Scherr, Violeta Petrescu, Santiago Martin Sondón and Johannes Sturm
Carinthia University of Applied Sciences

15:30 A Fully Integrated High-Voltage Charge Storing Gate Driver Supply for a 48-V DC-DC Converter
Dietmar Spiger and Bernhard Wicht
Leibniz University Hannover

15:50 On Demonstrating Beamforming Degradation from Translational Mounting Errors in a Coherent Radar Network
Martin Grünbacher, Mayeul Jeannin, Matthias Wagner and Mario Huemer
Infineon Technologies Austria AG, Johannes Kepler Universität Linz

16:10 Modeling Electrochemical Sensors with a Nonlinear Counter-Electrode Branch in Verilog-A
Christian Kogler, Emily Bezerra Alexandre, Tutku Beduk, Daniel Corzo, Christian Hambeck and Wolfgang Pribyl
Graz University of Technology, Infineon Technologies Austria AG, École polytechnique fédérale de Lausanne, Silicon Austria Labs GmbH

16:30 – 16:45 Conference Closing & Outlook Austrochip 2027

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